

(19) Japan Patent Office (JP)

(12) **KOKAI TOKKYO KOHO (A)**
[OFFICIAL GAZETTE FOR UNEXAMINED PATENT APPLICATIONS]

(11) Japanese Patent Application Kokai Publication Number: **H08-181309**

(43) Publication Date: July 12, Heisei 8 (1996)

(51) Int. Cl. ⁶	I.D. Code	JPO File No.	F I
H 01 L 29/78			
29/43			
		H 01 L 29/78	301 G
		29/62	Z

Examination Requested: Not yet requested
Number of Claims: 17 OL (11 pages in total) [Japanese text]

(21) Application Number: H06-319686
(22) Application Date: December 22, Heisei 6 (1994)
(71) Applicant: 000006013
Mitsubishi Electric Company [Mitsubishi Denki Kabushiki Kaisha]
2-3, Marunouchi 2-chome, Chiyoda-ku, Tokyo, Japan
(72) Inventor: Furukawa Akihiko
C/O Handotai Kiso Kenkyusho [Semiconductor Basics Research
Laboratory], Mitsubishi Denki Kabushiki Kaisha
1-1, Tsukaguchimoto-cho 8-chome, Amagasaki, Hyogo Prefecture,
Japan
(72) Inventor: Abe Yuji
C/O Handotai Kiso Kenkyusho, Mitsubishi Denki Kabushiki Kaisha
1-1, Tsukaguchimoto-cho 8-chome, Amagasaki, Hyogo Prefecture,
Japan
(74) Agent: Oiwa Masuo, patent attorney

(54) **TITLE OF THE INVENTION:**

Semiconductor device and a method of manufacturing the same

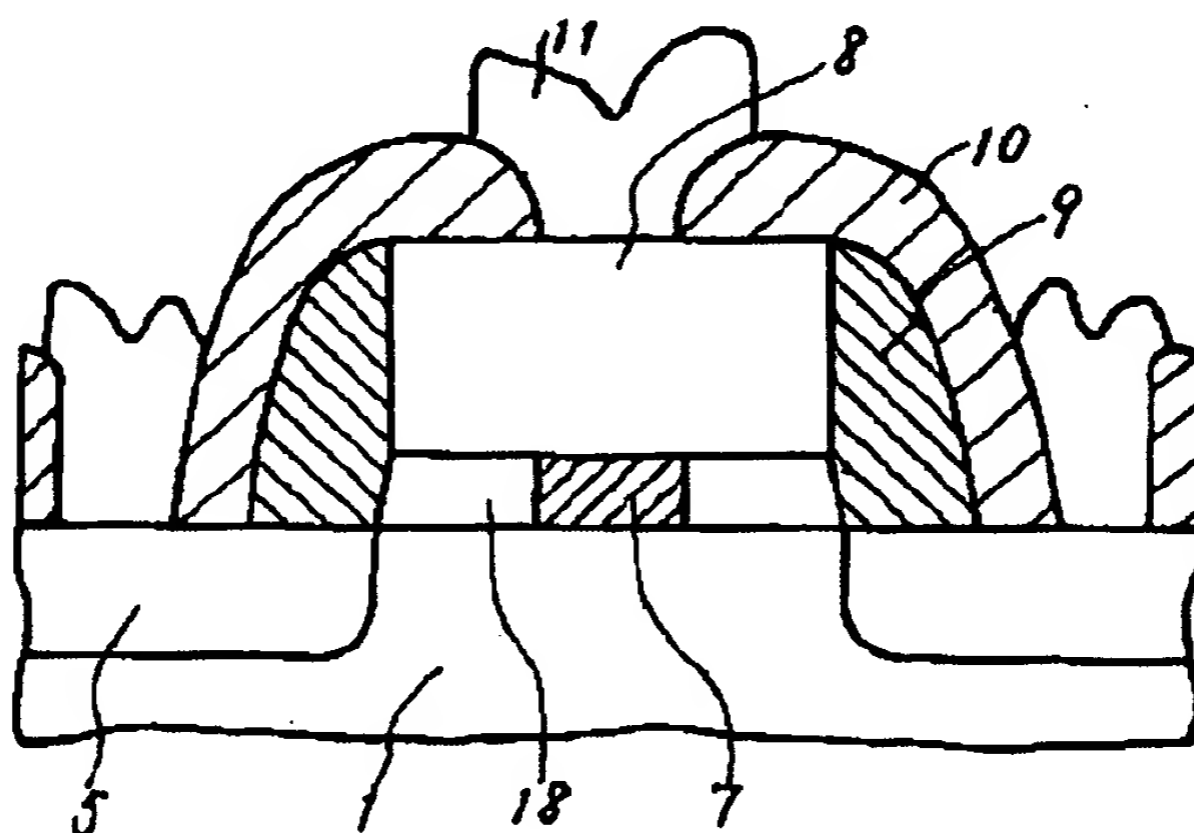
(57) **ABSTRACT**

PROBLEM TO BE SOLVED: To improve the reliability of the element by decreasing the electric field modulation at the edge of the gate electrode of the MOS semiconductor element and by reducing the degradation of its gate insulating film.

CONSTITUTION: A gate silicon oxide film 7 and polysilicon gate electrode 8 are formed on a silicon substrate 1 and, after a desired gate length is obtained by photoengraving, the gate

silicon oxide film 7 is made narrower by a method such as wet etching. A high-dielectric film 18 is then deposited in a manner so as to fill the space created under the polysilicon gate electrode 8 by the narrowing of the gate silicon oxide film 7, thereby forming a transverse (in the source-to-drain direction) gate insulating film comprised of the high-dielectric film 18, the silicon oxide film 7 and the high-dielectric film 18.

OPERATION: Providing the gate electrode virtually an inverted U-shaped structure results in the formation of a semiconductor element that is highly resistant to the short channel effect with hardly any increase in the number of fabrication steps.



- 1. Silicon substrate
- 5. High-concentration diffused layer
- 7. Gate silicon oxide film
- 8. Polysilicon gate electrode
- 9. Sidewall
- 18. High-dielectric film

CLAIMS

What is claimed is:

1. A semiconductor device having a gate electrode formed through the intermediary of a gate insulating film on the primary surface of the substrate, comprising a gate insulating film consisting of a plurality of layers of differing dielectric constants and oriented in a direction parallel to the primary surface of the substrate.
2. A semiconductor device according to claim 1, wherein the dielectric constant of at least the gate insulating film layer on the drain side at the edge of the gate is lower than that of the middle layer of the gate insulating film.
3. A semiconductor device according to claim 2, wherein:
 - the layer in the middle of the gate is a silicon oxide film; and
 - the layer on the drain side is hollow.
4. A semiconductor device according to claim 2, wherein:
 - the layer in the middle of the gate is a silicon oxide film; and
 - the layer on the drain side is a fluorosilicon oxide film.
5. A semiconductor device according to claim 2, wherein:
 - the layer in the middle of the gate is a silicone nitride film; and
 - the layer on the drain side is a silicon oxide film.
6. A semiconductor device according to claim 1, wherein the dielectric constant of the layers of the gate insulating film at the edges of the gate is higher than that of the layer in the middle of the gate.
7. A semiconductor device according to claim 6, wherein:
 - the layer in the middle of the gate is a silicon oxide film; and
 - the layer at the edges of the gate is a silicon nitride film or a barium strontium titanate film.

8. A semiconductor device, comprising:

a substrate having a primary surface;

a gate electrode formed in a manner so as to have both edges on an oxide film formed on the primary surface of the substrate in the area outside the active region and to have an air-bridge structure on the active region; and

a hollow gate insulating layer formed under the gate electrode.

9. A method of manufacturing a semiconductor device, comprising:

a step for forming a gate electrode on the primary surface of the substrate through the intermediary of a gate insulating film; and

a step for partially removing the gate insulating film by etching.

10. A method of manufacturing a semiconductor device according to claim 9, comprising a step for forming an insulating film on the sides of the gate insulating film and the gate electrode to create a cavity in the space from which the gate insulating film has been removed.

11. A method of manufacturing a semiconductor device, comprising:

a step for forming a gate electrode on the primary surface of the substrate through the intermediary of a gate insulating film;

a step for partially removing the gate insulating film by etching;

a step for forming a low-concentration diffused layer, by oblique ion implantation with rotation, under the space from which the gate insulating film has been removed; and

a step for creating a cavity in the space from which the gate insulating film has been removed by forming an insulating film on the sides of the gate insulating film and the gate electrode.

12. A method of manufacturing a semiconductor device according to claim 10 or claim 11, comprising a step for forming a passivation film consisting of a thin oxide film or a thin nitride film by rapid thermal processing.

13. A method of manufacturing a semiconductor device according to claim 9, comprising a step for filling the space from which the gate insulating film has been removed with a material having a low dielectric constant.

14. A method of manufacturing a semiconductor device according to claim 9, comprising a step for filling the space from which the gate insulating film has been removed with a material having a high dielectric constant.

15. A method of manufacturing a semiconductor device, comprising:

a step for forming a gate electrode through the intermediary of a gate insulating film on the primary surface of the substrate; and

a step for causing the gate insulating film at the edges of the gate to have a different dielectric constant from that of the gate insulating film in the middle of the gate by oblique ion implantation with rotation.

16. A method of manufacturing a semiconductor device according to claim 15, wherein the gate insulating film is a silicon oxide film, and comprising a step for turning the gate insulating film at the edges of the gate into a fluorine-doped silicon oxide film by oblique implantation with rotation using fluorine ions.

17. A method of manufacturing a semiconductor device, comprising:

a step for forming a gate electrode on the primary surface of a substrate through the intermediary of a gate-oxide film; and

a step for turning the gate oxide film at the edges of the gate to a nitrogen-doped silicon oxide film by oblique implantation with rotation using nitrogen ions.

DETAILED DESCRIPTION OF THE INVENTION

[0001]

Technical Field of the Invention: The present invention relates to a semiconductor device and a method of manufacturing the same, and, in particular, it relates to a constitution of an MOS field-effect transistor and a method of manufacturing the same.

[0002]

Description of Related Art: When attempting to microminiaturize an element, a thin gate insulating film and a shallow diffused layer with a depth of 0.1 μm or less needs to be formed if the MOS transistor is to be operated with a gate length in the 15 μm level. In the past, silicon oxide films were used for the gate insulating film. However, with advances in the microminiaturization of elements, silicon oxide films have become thinner, and a stronger electric field is applied on the gate insulating film, thereby putting the reliability of the oxide films into question. Consequently, the gate insulating film has been engineered lengthwise, with the result that those having a laminated structure comprised of silicon nitride and silicon oxide films are now used for this purpose. Because the dielectric constant of silicon nitride films is

about twice that of silicon oxide films, a laminate structure consisting of a silicon nitride film and a silicon oxide film yields 80 angstroms plus 20 angstroms for the total of 100 angstroms, whereas a silicon oxide film alone would be 60 angstroms. Therefore, lamination allows, at a first glance, for a thicker film design, thus making it possible to moderate the electric field.

[0003] As for the formation of the shallow junction, moreover, attempts have been made to reduce the energy of ion implantation and the temperature of heat treatment. Attempts to reduce the energy of the ion implantation made it necessary to carry out boron implantation at several KeV in order to form the shallow junction of the p-channel MOS (PMOS), and this led to the extreme degradation of process stability and throughput. Recently, reports about the use of solid-phase diffusion have started to appear. However, since these methods are merely the extensions of the prior art, there are still limitations with respect to the process. As for the junction whose depth is controlled by means of forming it electrically, instead of forming it by a process, there is a report of an element equipped with three built-in gate electrodes of its own 3, (a main gate with neighboring sub-gates, which moderate the electric field between the gate and the source) as shown in Fig. 15 (Hiromasa Noda et. al., IEDM, 1993, p.123).

[0004] In Figure 15, 1 is a silicon substrate, 2 a gate oxide film on the silicon substrate 1, 3 a main gate, 4 a sub-gate formed on the sides of the main gate 3 using an oxide film, and 5 a high-concentration diffused layer for the source/drain formed by ion implantation after the sub-gate 4 has been formed, while 6 is an inversion layer under the sub-gate. In Figure 15, the gate oxide film 2 and the main gate 3 are first formed on the silicon substrate 1. After the main gate 3 is patterned, the sub-gate 4 is formed. This is accomplished by forming an oxide film on the sides of the main gate 3 in order to prevent the sub-gate from shorting with the main gate 3. The high-concentration diffused layer for source/drain 5 is formed by ion implantation. Thus, an MOS semiconductor element is fabricated. The special feature of this transistor is found in that the junction depth of 0 μm is obtained because it uses the reverse charge of the silicon layer under the sub-gate 4 as a lightly doped drain (LDD) structure, even when it has basically the conventional single-drain structure wherein the low-concentration diffused layer has not been formed by such methods as ion implantation. To describe the operation of the transistor in more concrete terms, applying voltage (e.g., in the order of 10 V) on the sub-gate 4 in advance causes the inversion of the silicon layer underneath. The inversion layer 6 is very shallow, in the range of a score angstroms or so, and this area functions as the LDD layer of the common transistors. As a result, it obtains switching properties from the voltage applied on the main gate 3.

[0005]

Problems to be Solved by the Invention: With the prior art such as the ones described above, in other words, those having a laminate structure comprised of a silicon nitride film and an oxide film for moderating the electric field sustained by the gate insulating film, more time is needed to form the gate electrode, and there is a serious possibility that the interface characteristics will be compromised by the presence of an interface transition layer between the oxide and nitride film in the direction perpendicular to the electric current flow. This leads directly to the degradation of the element, as well as an increase in the number of steps required for its fabrication. Moreover, in the case the transistor that is designed to obtain a shallow junction, shown in Fig.

15, because three gates are set out in series in a manner so as to prevent them from shorting each other, each element requires a large flat space. Also there is the disadvantage that it requires a large number of fabrication steps.

[0006] The object of the present invention is to offer solutions to these two problems. In other words, it is to provide means for moderating the electric field on the gate oxide film 2 and for forming a shallow junction. As well, it is to fabricate the element using a simple process and to offer process steps that are not in anyway inferior to the usual process employed to form the MOS semiconductor element.

[0007]

Means for Solving the Problems: The semiconductor device relating to the present invention is provided with a gate insulating film comprised of a plurality of layers of differing dielectric constants oriented in a direction parallel to the primary surface of the substrate. Moreover, the layer of the gate insulating film at the edge of the gate, at least on the drain side, is provided with a dielectric constant lower than that of the layer in the middle of the gate. [In one aspect of the invention,] a silicon oxide film serves as the layer in the middle of the gate, whereas the layer on the drain side is made into a cavity. [In another aspect of the invention,] a silicon oxide film is used to serve as the layer in the middle of the gate, whereas a fluorosilicon oxide film is used for the layer on the drain side. [In another aspect of the invention,] a silicon nitride film is used for the layer in the middle of the gate, while a silicon oxide film is used for the layer on the drain side. [In another aspect of the invention,] the layer of the gate insulating film at the edge of the gate is provided with a dielectric constant higher than that of the layer in the middle of the gate. [In yet another aspect of the invention,] a silicon nitride film is used for the layer in the middle of the gate, while a silicon nitride film or a barium strontium titanate film is used for the layer at the edge of the gate. Moreover, the semiconductor device of the present invention is provided with a gate electrode, which is formed on the primary surface of the substrate in a manner so as to have both edges on the part of the oxide film lying outside the active region and to form an air-bridge structure over the active region, and a hollow gate insulating film formed under the gate electrode.

[0008] Furthermore, the method of manufacturing a semiconductor device relating to the present invention includes a step for forming a gate electrode on the primary surface of a substrate through the intermediary of a gate insulating film and a step for removing parts of the gate insulating film by etching. It also includes a step for forming a cavity in the space left behind by the removed portion of gate insulating film by forming a insulating film on the sides of the gate insulating film and the gate electrode. [In another aspect of the invention,] it includes a step for forming a gate electrode on the primary surface of the substrate through the intermediary of a gate insulating film, a step for removing parts of the gate insulating film by etching, a step for forming by oblique ion implantation with rotation a low-concentration diffused layer under the area from which the gate insulating film has been removed, a step for forming an insulating film on the sides of the gate insulating film and the gate electrode, and a step for creating a cavity in the space from which the gate insulating film has been removed. Furthermore, it includes a step for forming a passivation film, which consists of a thin oxide film

or a thin nitride film, in the cavity of the gate insulating film by rapid thermal processing. It also includes a step for filling the space from which the gate insulating film has been removed with a material having a low dielectric constant.

[0009] Moreover, it includes a step for filling the space from which the gate insulating film has been removed with a material having a high dielectric constant. In addition, it includes a step for forming a gate electrode on the primary surface of a substrate through the intermediary of a gate insulating film and a step for carrying out oblique ion implantation with rotation so as to give the gate insulating film at the edge of the gate a dielectric constant different from that of the gate insulating film in the middle of the gate. It also contains a step for turning the gate insulating film comprised of a silicon oxide film at the edge of the gate into a fluorine-doped silicon oxide film by carrying out

oblique injection with rotation using fluorine ions. Moreover, it includes a step for forming a gate electrode on the primary surface of a substrate through the intermediary of a gate oxide film and a step for turning the gate oxide film at the edge of the gate to a nitrogen-doped silicon oxide film by oblique implantation using nitrogen ions.

[0010]

Operation: With the above described semiconductor device or the method of manufacturing the same, the device is constructed in a manner so that the layer of the gate insulating film at the edge of the gate, at least on the drain side, has a lower dielectric constant than the layer in the middle of the gate, causing the gate electric field to take on a virtual T-shape. Moreover, the layer of the gate insulating film at the edge of the gate is made to have a higher dielectric constant than the layer in the middle of the gate, and the gate electric field to form a virtual U-shape, so that, when low voltage is applied on the gate, the silicon under the high-dielectric film is reversed and forms an inversion layer, which is a shallow junction, to function as the LDD. Moreover, the device is provided with a gate electrode, both edges of which are placed outside the active region on the primary surface of the substrate to form an air-bridge structure, and a hollow gate insulating film, which is formed under the gate electrode, with the edge of the gate being the gate insulating film of a low dielectric constant.

[0011] Moreover, the manufacturing method includes a step for forming a gate electrode through the intermediary of a gate insulating film on the primary surface of the substrate and a step for partially removing the gate insulating film by etching, thus allowing for the gate insulating film at the edge of the gate to be formed into separate parts. Moreover, it contains a step for creating a cavity in the space left behind by the removed gate insulating film by forming an insulating film on the sides of the gate insulating film and the gate electrode, to yield a gate electric field having a virtual T-shape. Moreover, the manufacturing method includes the following: a step for forming a gate electrode on the primary surface of the substrate through the intermediary of a gate insulating film; a step for partially removing the gate insulating film by etching; a step for forming, by oblique ion implantation with rotation, low-concentration diffused layer under the area from which the gate insulating film has been removed; a step for forming an insulating film on the sides of the gate insulating film and the gate electrode and for creating a cavity from the space from which the gate insulating film has been removed, resulting in a gate

electric field having a virtual T-shape and thereby providing an effective gate length shorter than the length of the gate electrode.

[0012] Furthermore, a passivation film, comprised of a thin oxide or nitride film, is formed in the cavity of the gate insulating film by rapid thermal processing. In addition, the manufacturing method of the present invention includes a step for forming a gate electrode on the primary surface of the substrate through the intermediary of a gate insulating film and a step for causing the gate insulating film at the edge of the gate to have a dielectric constant different from that of the gate insulating film in the middle of the gate by oblique ion implantation with rotation, with a result that the gate insulating film at the edge of the gate can be made to have either a high or a low dielectric constant. Moreover, the gate insulating film is comprised of a silicon oxide film, and the method also includes a step for turning the gate insulating film at the edge of the gate into a fluorine-doped silicon oxide film by oblique implantation with rotation using fluorine ions, resulting in a gate electric field having a virtual T-shape. Moreover, the manufacturing method includes a step for forming a gate electrode on the primary surface of the substrate through the intermediary of a gate oxide film and for turning the gate oxide film at the edge of the gate into a nitrogen-doped silicon oxide film by oblique implantation with rotation using nitrogen ions, so that the gate electric field forms a virtual inverted U-shape when gate voltage is applied.

[0013]

Description of the Preferred Embodiments

Example 1: Fig. 1 is a block diagram of the relevant parts of an MOS semiconductor element, while Fig. 2 is a block diagram showing the shape of a virtual gate insulating film obtained by the conversion of a silicon oxide film. In the diagram, since 1 and 5 are the same as those of the conventional device, explanation thereof will be omitted. In Fig. 1, 7 is a gate silicon oxide film constituting a part of the gate insulating film, 8 a polysilicon gate electrode formed on the gate insulating film, 9 a sidewall comprised of a silicon nitride film or a [silicon] oxide film formed on the sides of the polysilicon gate electrode 8, 10 a protective film covering the entire semiconductor element, and 11 an aluminum electrode used as a contact. Furthermore, 12 is a low-concentration diffused layer formed on a silicon substrate 1, while 13 is a hollow structure, which is either vacuum or air-filled, formed in between the gate silicon oxide film 7 and the sidewall 9.

[0014] In Figure 2, 14 is a virtual gate electrode having a T-shaped structure, 15 a virtual gate silicon oxide film having a U-shape structure. With this MOS semiconductor element, as shown in Fig. 1, the gate insulating film on the silicon substrate 1 is built of transversely oriented (in the direction of a source-to-drain channel) three components: a vacuum or air-filled hollow structure 13, a gate silicon oxide film 7 and a vacuum or air-filled hollow structure 13. In other words, it has a transversely oriented three-ply laminate structure (Generally, lamination means stacking in a vertical direction. However, this is not the case here.) The method of manufacturing an MOS semiconductor element according to Example 1 of the present invention will be described next with reference to Fig. 1. A well (not shown in the diagram) is formed on the MOS silicon substrate 1 according to a commonly used process for fabricating an MOS

element, followed by a step for forming a gate silicon oxide film 7 functioning as a gate insulating film and a polysilicon gate electrode 8. A desired gate length is then obtained by photoengraving. Next, the gate silicon oxide film 7 is made narrower (partially removed) by wet-etching using a substance such as hydrofluoric acid. After a low-concentration diffused layer 12 is formed, a sidewall 9 is formed using a silicon nitride or oxide film. During the formation of the sidewall 9, a part of the space between the silicon substrate 1 and the polysilicon gate electrode 8 takes on a hollow structure to form, in a transverse direction, a vacuum or air-filled hollow structure 13, a gate silicon oxide film 7 and another vacuum or air-filled hollow structure 13. Furthermore, a source/drain high-concentration diffused layer 7 is also formed. A protective film 10 is then deposited on the entire surface of the element, and a contact for each region is made by means of materials such as an aluminum electrode 11 to obtain a finished MOS semiconductor element.

[0015] The step for narrowing the gate silicon oxide film 7 may be performed using reactive dry etching (RIE) in order to obtain improved accuracy than that obtained by wet etching. Moreover, prior to the step using wet etching, carrying out the deposition of a silicon nitride film, tungsten or other materials after the formation of the polysilicon electrode 8 will serve to prevent the collapse or distortion of the polysilicon electrode 8 after the gate silicon oxide film 7 is narrowed. In this symmetrical MOS semiconductor element whose gate insulating film is comprised of three transversely laminated layers, the dielectric constant of the hollow structure 13 is roughly 1, since it contains near vacuum, or air at reduced pressure or at atmospheric pressure, whereas the dielectric constant of the gate silicon oxide film 7 is 3.9. Because of this dielectric constant, when considered as if there were only a silicon oxide film*, the thickness of the film in the hollow structure 13 would be about four times that of the gate silicon oxide film 7. As a result, the virtual gate electrode (shape indicating the gate electric field intensity at the time of the application of the gate voltage) 14 takes on a virtually T-shaped structure (in the case of the virtual gate silicon oxide film 15, a virtually U-shaped structure), as shown in Fig. 2. For this reason, the moderation of the intense electric field created between the drain and the gate can be achieved in conventional MOS elements, thus improving their reliability.

[0016] Moreover, the low dielectric film near the edge of the gate insulating film poses a risk of causing a decline in the current driving capacity. This can be avoided by providing the low-concentration diffused layer with a gate overlap structure. Example 1 was described with respect to the MOS semiconductor element of a type that is symmetrical on both the source and drain sides. However, it is also possible to reduce the dielectric constant of the gate insulating film near the drain alone.

[0017] Example 2: In Example 1, hollow structures 13 were set up in parts of the gate insulating film. In the case of Example 2, however, after the gate silicon oxide film 7 and polysilicon gate 8 have been formed and the gate silicon oxide film 7 made narrower, a substance having a different dielectric constant, especially the fluorosilicon oxide of the low-

* Translator's note: Probable meaning.

dielectric film, is deposited and subjected to the etch-back process to fill the space underneath the polysilicon electrode 8. As a result, a gate insulating film comprised of a fluorosilicon oxide film, a silicon oxide film and a fluorosilicon oxide film, all transversely oriented, is formed. This makes it possible to moderate the electric field at the edges of the gate generated as a result of the electric field concentration there, thereby serving to extend the life expectancy of the element. Moreover, a silicon nitride film may be used for the gate insulating film. In this case, a gate insulating film consisting of a silicon oxide film, a silicon nitride film and a silicon oxide film, all arranged transversely, is obtained by depositing a silicon oxide film on the silicon nitride film after it is made narrower.

[0018] Example 3: After the gate silicon oxide film 7 and polysilicon gate electrode 8 are formed according to Example 1, the gate silicon oxide film 7 in the active region is narrowed down by isotropic etching, and its surface is then slightly oxidized or nitridized by rapid thermal processing (RTP) in an N_2 environment at 800°C to 1,000°C for about 30 seconds, to yield a passivation film. The passivation film on the source/drain is then removed by anisotropic etching to form a contact for the drain/source. The defects generated during the step for narrowing the gate oxide film 7 are removed by the passivation film, thus providing improved resistance to degradation caused by the injection of carriers into the gate at gate edges.

[0019] Example 4: Fig. 3 is a block diagram illustrating the relevant parts of an MOS semiconductor element according to Example 4 of the present invention, while Fig. 4 is a plan view showing a block diagram of an MOS semiconductor element according to Example 4 of the present invention. In this example, after a gate silicon oxide film 7, a polysilicon gate electrode 8 and a silicon nitride film or tungsten are formed, all of the gate silicon oxide film 7 lying in the active region is removed by isotropic etching. Here, the pattern for the polysilicon gate electrode 8 is shaped in a manner so as to have the gate length outside the active region longer than that in the active region. To put it more concretely, the pattern is made to have the shape shown in Fig. 4. This makes it possible to leave untouched the parts of the gate silicon oxide film 7 lying outside the active region and to form a gate insulating film 16 having an air-bridge structure and comprised of a vacuum or air. Then, the step for forming the sidewall is carried out, to obtain a finished MOS semiconductor element having a gate insulating film comprised of vacuum or air. Breakdown caused by defects generated by hot carriers and the like in the gate insulating film having the conventional structure generally takes place at the edge of the gate on the drain side. Whereas the gate insulating films of the conventional structure are associated with degradation, the present invention provides a gate oxide film which is ideally free of near-traps, thereby providing a defect-free element. However, because its dielectric constant is low and its current driving capacity reduced, the thickness of the insulating film must be several nanometers.

[0020] Example 5: In this example, oblique implantation with rotation is carried out using fluorine ions after the formation of the gate insulating film, which is a silicon oxide film, and the polysilicon gate electrode. The fluorine used is implanted into the silicon oxide film near the edges of the gate electrode, and an appropriate heat treatment is carried out to yield a fluorine-doped silicon oxide film (SiOF) having a low dielectric constant. Because this results in the

electrode's edges, where electric field concentration takes place, to have low dielectric constants, the electric field can be moderated, as was the case in Example 1, thus extending the life expectancy of the element. Moreover, because fluorine, which is implanted into the silicon of the silicon substrate and the polysilicon gate electrode, suppresses the diffusion of similar semiconductor impurities such as boron, this eliminates the need to implant fluorine in a separate step.

[0021] Example 6: Fig. 5 is a block diagram illustrating the relevant parts of an MOS semiconductor element according to Example 6 of the present invention, while Fig. 6 is a block diagram illustrating the shape of a virtual gate insulating film in terms of a silicon oxide film. Fig. 7 is a block diagram illustrating the MOS in operation when a low gate voltage is applied, while Fig. 8 is a block diagram illustrating the MOS in operation when a high gate voltage is applied. After a gate silicon oxide film 7 and a gate electrode are formed and the gate silicon oxide film 7 is narrowed, a dielectric substance with a different dielectric constant, in particular, a high-dielectric film 18, is deposited, and the commonly used etch-back process is carried out to fill the space underneath the gate electrode. In cases where the film is very thin, ammonia or the like is introduced to serve as a gas ingredient, and a nitridation treatment is carried out on the gate polysilicon and the silicon substrate using RTP, to obtain a gate silicon nitride film. In this manner, The fill material comprising the high-dielectric film 18 on the side of the source or the drain and the narrowed gate silicon oxide film 7 are used to form a symmetrical MOS semiconductor element. Films that can be used for the high-dielectric film 18 includes silicon nitride films, barium strontium titanate (BST) film and the like. When considered as if this consists only of a silicon oxide film*, as was the case with Example 1, it means that a virtual gate electrode 19 has a virtual inverted U-shape structure (a virtual gate silicon oxide film 20), as shown in Fig. 6.

[0022] This results in the high-dielectric film 18 having a relatively stronger electric field than the gate silicon oxide film 7. Under the conditions shown in Fig. 7 while a low voltage is applied on the gate, the silicon under the high-dielectric film 18 undergoes inversion to form an inversion layer 21. This inversion charge is used as the LDD structure of the low-concentration diffused layer. It is a two-dimensional inversion layer, and this means that a very shallow junction is formed. Next, as the voltage applied on the gate electrode is raised, the silicon underneath the gate silicon oxide film 7 undergoes inversion to form an inversion layer 22, and this causes the current to flow. The switching properties of the transistor are controlled by the silicon underneath the gate silicon oxide film 7. The operation of the transistor is basically similar to that shown in the example of the conventional transistor. However, the operation of the transistor of the present invention is controlled by one gate alone. As compared with transistors having the usual single-drain structure, the transistor of the present invention provides a means for shortening the effective gate length (L_{eff} [gate length]), thus providing enhanced current driving capacity. This is an MOS semiconductor element having a very shallow junction, it is an MOS element structure that is highly resistant to the short channel effect.

* Translator's note: Probable meaning; the exact meaning of this phrase is unclear.

[0023] Example 7: Fig. 9 is a block diagram illustrating a fabrication method for an MOS semiconductor element according to Example 7 of the present invention. The steps used for manufacturing are basically the same as those described in Example 5. In Example 7, however, nitrogen is oblique implanted 23 into the gate silicon oxide film 7 in the area lying near the edge of the gate electrode. By carrying out appropriate heat treatment, the gate silicon oxide film 7 near the edge is turned into a nitrogen-doped silicon oxide film 24 having a higher dielectric constant than that of the oxide film, thus providing the same effects as those achieved by Example 6. Moreover, nitrogen 25 implanted into the gate electrode has the effect of suppressing the diffusion of boron and other impurities in the semiconductor, thereby eliminating the need to carry out nitrogen implantation in a separate step. Moreover, nitrogen 26 implanted into the source/drain high-concentration layer is expected to have a similar effect, so this does not pose a problem. Moreover, the present invention uses the usual process of manufacturing elements, so there is hardly any increase to the number of steps required.

[0024] Next, the MOS semiconductor element described in examples 6 and 7 were examined by comparing their transistor performance with that of the conventional single-drain and the gate-overlap LDD structures by simulation. The results thus obtained will be described hereinafter. Fig. 10 is a schematic drawing of an MOS semiconductor element used in simulation. The single-drain structure is shown in (a), the gate-overlap LDD structure in (b) and the structure according to the present invention in (c). The numeric references 5, 7, 8, and 18 are the same as those of Fig. 5, and 12 is a low-concentration diffused layer. The gate silicon oxide film 7 (dielectric constant of 3.9) and the gate high-dielectric film 18 (dielectric constant of 10.0) were assigned a rectangular shape. The values assigned were as follows: A = 0.27 μm , B = 0.2 μm , C = 0.452 μm , D = 0.008 μm , E = 1.0 μm , F = 0.1 μm , G = 0.25 μm , H = 0.05 μm and I = 0.15 μm . The concentrations of impurities were set as follows: $1 \times 10^{20} \text{ cm}^{-3}$ for the source/drain high-concentration layer, $1 \times 10^{18} \text{ cm}^{-3}$ for the low-concentration diffused (LDD) layer, and the substrate concentration of $3 \times 10^{17} \text{ cm}^{-3}$.

[0025] Fig. 11 shows the electric current voltage properties obtained by the simulation of MOS semiconductor elements, where (a), (b) and (c) correspond to the structures shown in Fig. 10. When the voltage applied was 2.5 V for the gate electrode, 2.5 V for the drain and -1.0 V for the substrate, the following drain current was obtained: (a) 4.94 mA for the single-drain structure, (b) 5.48 mA for the gate-overlap LDD structure, and (c) 5.21 mA for the structure according to the present invention. The effective gate length being shorter than that of others by about 0.1 μm is responsible for the higher current driving capacity of the gate-overlap LDD structure. When the dielectric constant of the gate high-dielectric film 18 of the structure according to the present invention was set at 10, it was found that the drain current obtained was about 5% higher than that obtained for the single-drain structure. Furthermore, when the dielectric constant of the high-dielectric film 18 was set at around 20, it was found that the current driving capacity obtained was at the same level as that obtained for the gate-overlap LDD structure.

[0026] Fig. 12 shows the potential distribution curves obtained by simulation, where (a), (b) and (c) correspond to the structures shown in Fig. 10. When the voltage applied was 0.0 V for the gate, 2.5 V for the drain and -1.0 V for the substrate, it was found that the potential from the

drain flared out greatly near the surface in the case of the gate-overlap LDD structure (b), i.e., the hollow layer of the drain was greatly stretched, thus allowing for punch through to take place easily. In the case of the structure according to the present invention (c), on the other hand, the results obtained were similar to those obtained for the single-drain structure (a), demonstrating that it is resistant to punch through of the surface. Fig. 13 shows the relationship between transversely oriented (in the source-to-drain direction) electric field and potential obtained by simulation, where (a), (b) and (c) correspond to the structures shown in Fig. 10. When the voltage applied was 2.5 V for the gate, 2.5 V for the drain and 1.0 V for the substrate, it was found that the transverse electric field on the drain side was suppressed for both the gate-overlap LDD structure (b) and the structure of the present invention (c). When the results shown in Fig. 11 to Fig. 13 were compiled, it was found that, with the structure of the present invention having a high-dielectric film as the gate insulating film on the drain side, the transverse electric field was moderated and this resulted in enhanced current driving capacity, as was the case with the LDD structure. At the same time the present invention was resistant to punch-through which is a weakness of the LDD structure

[0027] Example 8: Fig. 14 is a block diagram showing the pertinent parts of an MOS semiconductor element according to Example 8 of the present invention. The method of manufacturing the MOS semiconductor element relating to Example 8 will be described next. A gate electrode of the desired length is formed on a silicon substrate 1 by a commonly used fabrication process for an MOS semiconductor element. For example, a gate electrode length 27 of $0.3\ \mu\text{m}$ is formed. The gate insulating film, e.g., a gate silicon oxide film 7, is then narrowed down by removing $0.1\ \mu\text{m}$ from each edge, for example. The bottom of the narrowed silicon gate oxide film 7, width of $0.1\ \mu\text{m}$, becomes the effective gate length 28 of the transistor. A low-concentration diffused layer 12 is formed under the hollow structure 13 of the gate insulating film by oblique implantation 29 with rotation. When a sidewall 9 is formed in a similar manner, a hollow structure is created between the silicon substrate 1 and parts of the polysilicon gate electrode 8, to form, in a transverse direction, a hollow structure comprised of a vacuum 13, a silicon oxide film 7 and another hollow structure comprised of a vacuum 13. In this MOS semiconductor device, the effective gate length 28 can be shorter than the gate electrode length 27, for example, in the order of $L_{\text{eff}} = 0.1\ \mu\text{m}$ and $L_g = 0.3\ \mu\text{m}$, so that increase in the gate resistance can be prevented by sub-quarter micron.

[0028]

Advantages of the Invention: Because the present invention is constituted in the manner described above, it provides the following advantages. Giving the layer of the gate insulating film at the edge of the gate, at least on the drain side, a lower dielectric constant than that of the layer in the middle creates a virtual T-shaped gate electric field when the gate voltage is applied. As a result, the concentration of electric field at the edge of the gate electrode that can greatly affect the deterioration of the MOS semiconductor element can be moderated, resulting in improved life expectancy of the element. Moreover, giving the layer of the gate insulating film at the edges of the gate a higher dielectric constant than that of the middle layer creates a virtual inverted U-shape gate electric field. As a result, when low voltage is applied on the gate, the silicon under the high-dielectric layer is inverted to form an inversion layer, which is a shallow

junction. Because this layer acts as an LDD, an MOS semiconductor element having a shallow junction is obtained. As a result, the fabrication of an element that is highly resistant to the short-channel effect is possible. As well, the element is highly resistant to punch through, which is a disadvantage of the LDD structure, and offers enhanced current driving capacity.

[0029] Moreover, the device of the present invention is provided with a gate electrode, which is formed with both its edges on the part of the oxide film formed on the primary surface of the substrate, in the area outside the active region to form an air-bridge structure over the active region and a hollow gate insulating film formed under the gate electrode. Furthermore, because the edges of the gate insulating film have low dielectric constants, degradation of the gate insulating film caused by hot carriers is eliminated. Furthermore, the manufacturing method of the present invention includes a step for forming a gate electrode on the primary surface of the substrate through the intermediary of a gate insulating film 7 and a step for partially removing the gate insulating film by etching, to divide the gate insulating film into separate parts. As a result, there is hardly any increase in the number of steps required, so fabrication is inexpensive.

[0030] Moreover, it includes a step for creating a cavity in the space from which the gate insulating film has been removed, which is accomplished by forming an insulating film on the sides of the gate insulating film and the gate electrode. As a result, the gate electrode takes on a virtual T-shape, and this makes it possible to moderate the concentration of electric field at the edge of the gate electrode. Moreover, it also includes: a step for forming a gate electrode through the intermediary of a gate insulating film; a step for partially removing the gate insulating film by etching; and a step for forming, by oblique ion implantation with rotation, a low-concentration diffused layer under the space left by the removal of the gate insulating film. It also includes a step for creating a cavity from the space left behind by the removal of the gate insulating film by forming an insulating film on the sides of the gate insulating film and the gate electrode. As well, the gate electrode takes on a virtual T-shaped structure having an effective gate length that is shorter than the gate electrode length. Therefore, an increase in the gate resistance can be prevented by sub-quarter micron.

[0031] Furthermore, a passivation layer of a thin oxide or nitride film is formed in the middle of the gate insulating film by rapid thermal processing, the defects, which are produced during the step for the partial removal of the gate insulating film, can be eliminated by the passivation film. Because this prevents the degradation that takes place at the edge of the gate electrode due to hot carriers injected into the gate, it serves to extend the life expectancy of the element. Moreover, the method includes a step for forming a gate electrode on the primary surface of the substrate through the intermediary of a gate insulating film and a step for causing the edge of the gate insulating film to have a different value of dielectric constant than that of the middle of the gate insulating film. Therefore, the edge of the gate insulating film can be made to have either a high or a low dielectric constant, with a result that there is hardly any increase in the number of steps required. This, in turn, leads to a low cost of fabrication.

[0032] Moreover, the method of the present invention uses a silicon oxide film for the gate insulating film and includes a step for turning the edge of the gate insulating film into a fluorine-

doped silicon oxide film by carrying out oblique implantation with rotation using fluorine ions, to form a gate electrode having a virtual T-shaped structure. This makes it possible to moderate the electric field and improve the life expectancy of the element. Since this method involves hardly any increase in the number of steps required, the cost of fabrication is low. Moreover, the method includes a step for forming a gate electrode on the primary surface of the substrate through the intermediary of a gate oxide film, and a step for turning the parts of the gate oxide film at the edge of the gate into a nitrogen-doped silicon oxide film by performing oblique implantation with rotation using nitrogen ions to form a gate electrode having a virtual inverted U-shape. This makes it possible to moderate electric field and improve the life expectancy of the element. Since this method involves hardly any increase in the number of steps required, it is possible to obtain an MOS semiconductor element having a shallow junction at a low cost. As well, the method provides an element that is highly resistant to punch through and has an improved current driving capacity.

Brief Description of the Drawings

Fig. 1 is a block diagram illustrating the relevant parts of an MOS semiconductor element according to Example 1 of the present invention.

Fig. 2 is a block diagram illustrating the virtual electrode and insulating film of an MOS semiconductor element according to Example 1 of the present invention.

Fig. 3 is a block diagram illustrating the relevant parts of an MOS semiconductor element according to Example 4 of the present invention.

Fig. 4 is a plan view illustrating an MOS semiconductor element according to Example 4 of the present invention.

Fig. 5 is a block diagram illustrating the relevant parts of an MOS semiconductor element according to Example 6 of the present invention.

Fig. 6 is a block diagram illustrating the virtual electrode and insulating film of an MOS semiconductor element according to Example 6 of the present invention.

Fig. 7 is a block diagram illustrating the operating method of an MOS semiconductor element while under the application of a low gate voltage according to Example 6 of the present invention.

Fig. 8 is a block diagram illustrating the operating method of an MOS semiconductor element while under the application of a high gate voltage according to Example 6 of the present invention.

Fig. 9 is a block diagram illustrating a method of fabricating an MOS semiconductor element according to Example 7 of the present invention.

Fig. 10 is a schematic drawing illustrating the structures used for simulation according to Example 7 of the present invention.

Fig. 11 is a graph showing the electric current and the voltage properties obtained by simulation of MOS semiconductor elements according to Example 7 of the present invention.

Fig. 12 is a graph showing potential distribution curves obtained by simulation of MOS semiconductor elements according to Example 7 of the present invention.

Fig. 13 is a graph showing the relationship of the transverse (in the source-to-drain direction) electric field with the potential of an MOS semiconductor element according to Example 7 of the present invention.

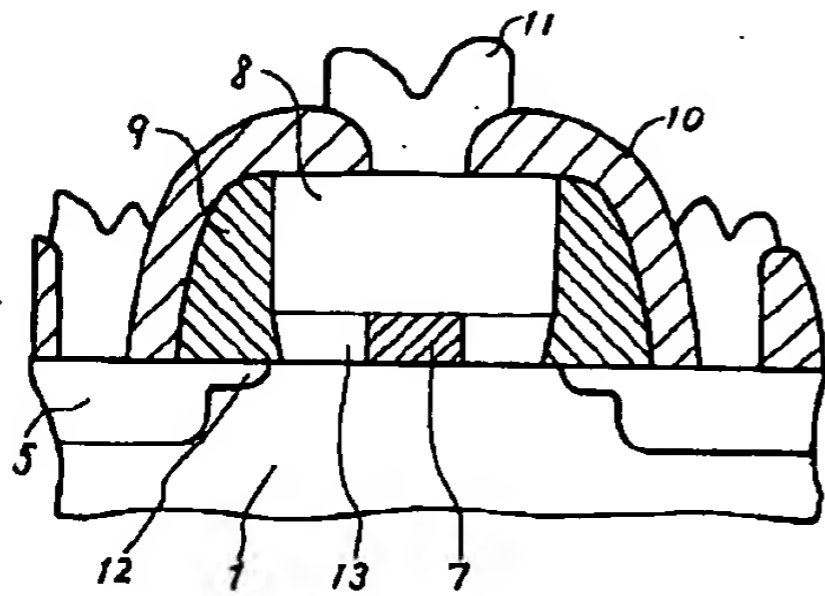
Fig. 14 is a block diagram illustrating the relevant parts of an MOS semiconductor element according to Example 8 of the present invention.

Fig. 15 is a block diagram illustrating the relevant parts of a conventional MOS semiconductor element.

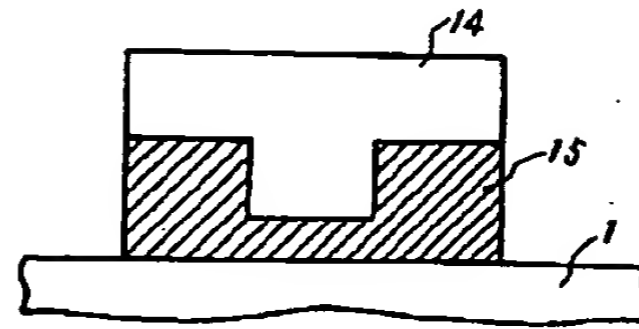
Description of the Reference Numerals

- 1 Silicon substrate
- 5 High-concentration diffused layer
- 7 Gate silicon oxide film
- 8 Polysilicon gate electrode
- 9 Sidewall
- 10 Protective film
- 11 Aluminum electrode
- 12 Low-concentration diffused layer
- 13 Hollow structure
- 14 & 19 Virtual gate electrode
- 15 & 20 Virtual gate silicon oxide film
- 16 Vacuum (air) gate insulating film
- 18 High-dielectric film
- 21 Inversion layer induced under the high-dielectric film
- 22 Inversion layer induced under the silicon oxide film
- 24 Nitrogen-doped silicon oxide film
- 27 Gate electrode length
- 28 Effective gate length

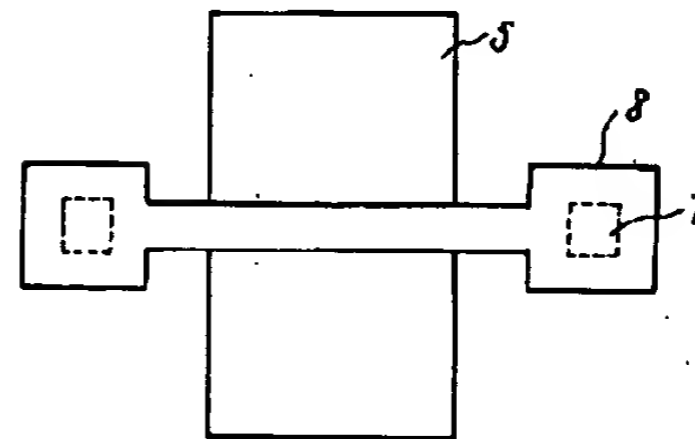
【図1】



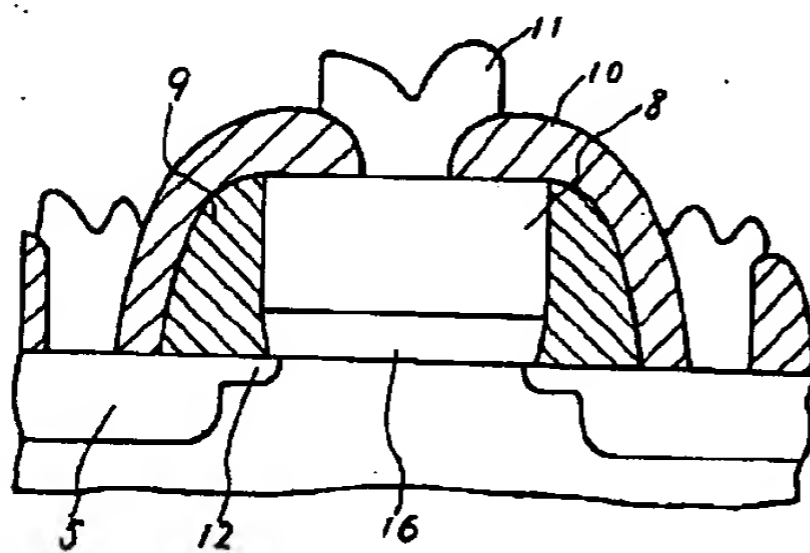
【図2】



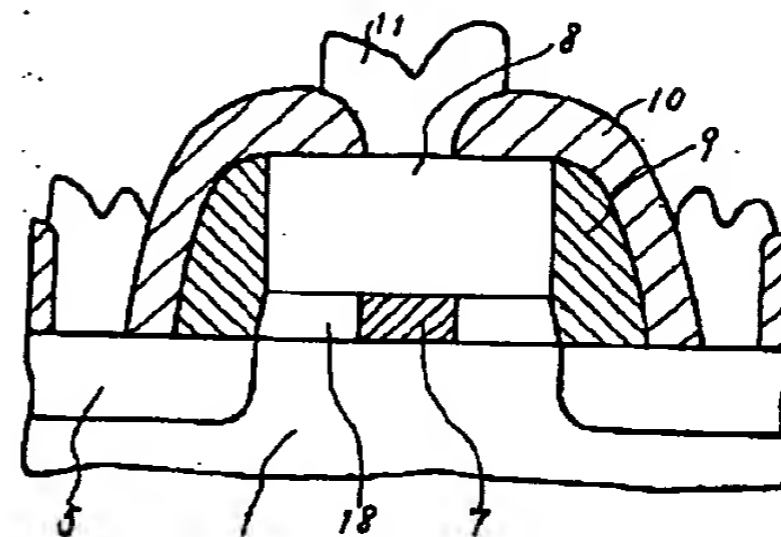
【図4】



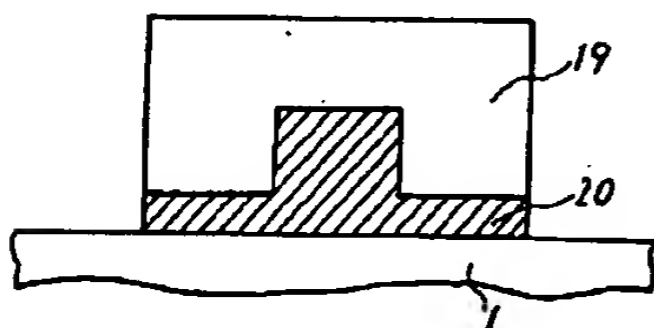
【図3】



【図5】

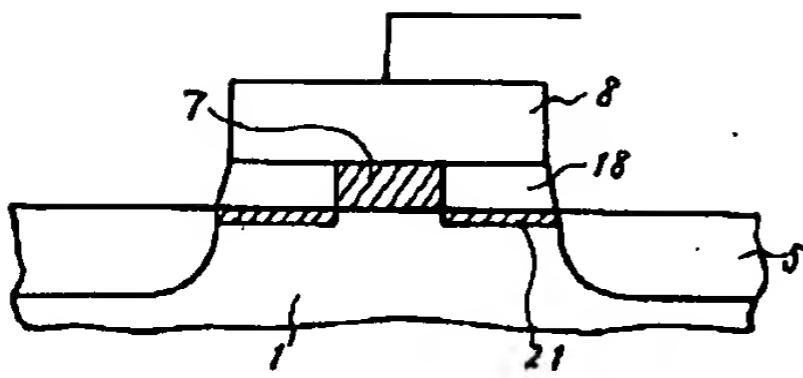


【図6】

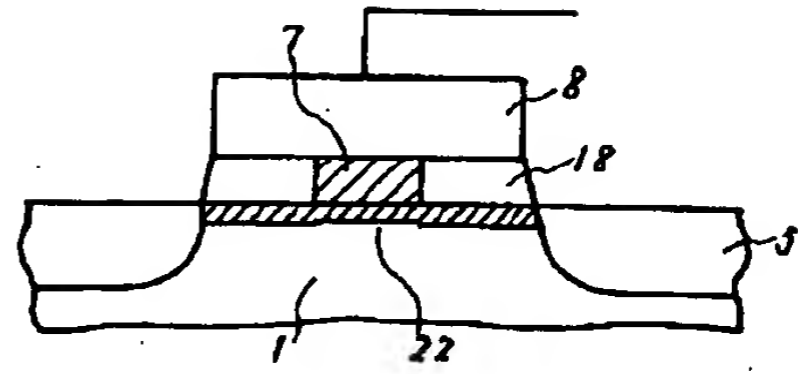


- 1 Silicon substrate
- 5 High-concentration diffused layer
- 7 Gate silicon oxide film
- 8 Polysilicon gate electrode
- 9 Sidewall
- 18 High-dielectric film

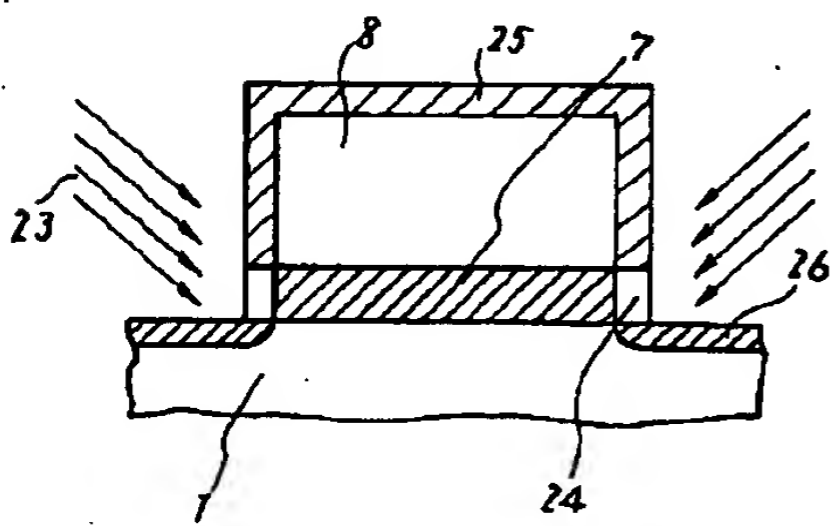
【図7】



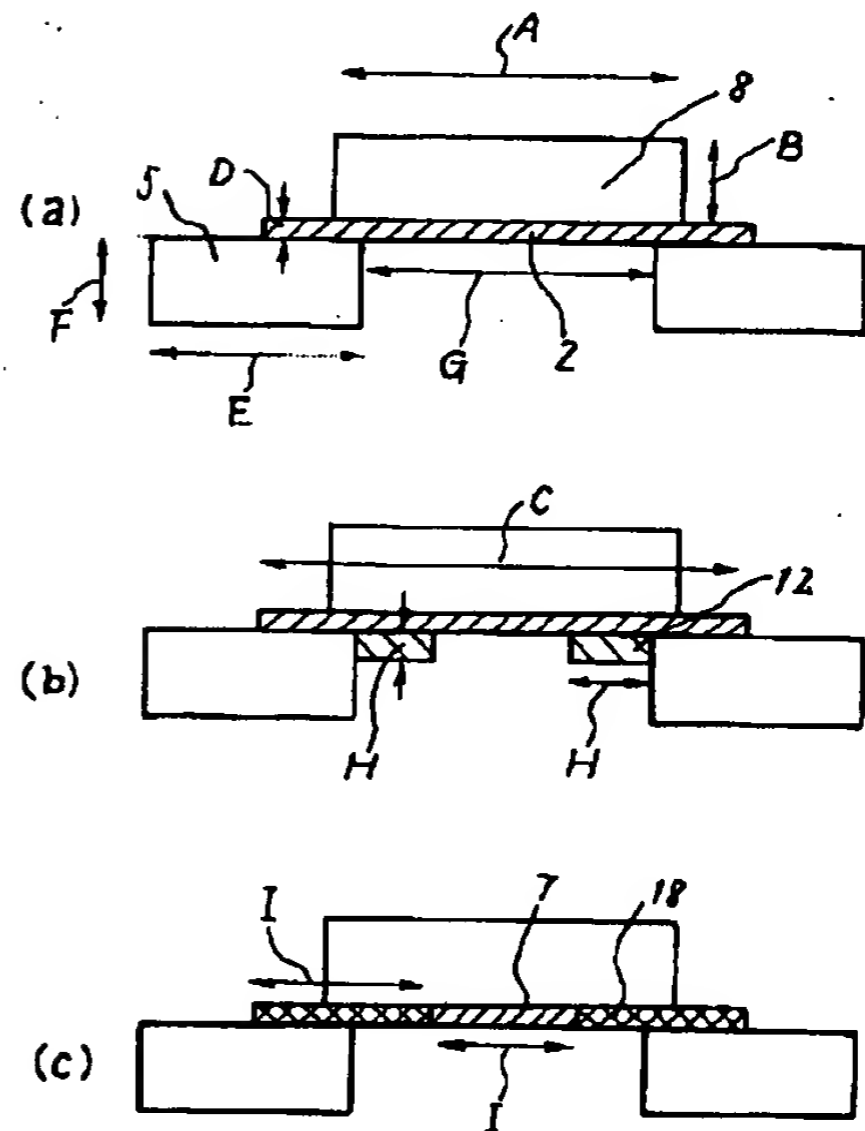
【図8】



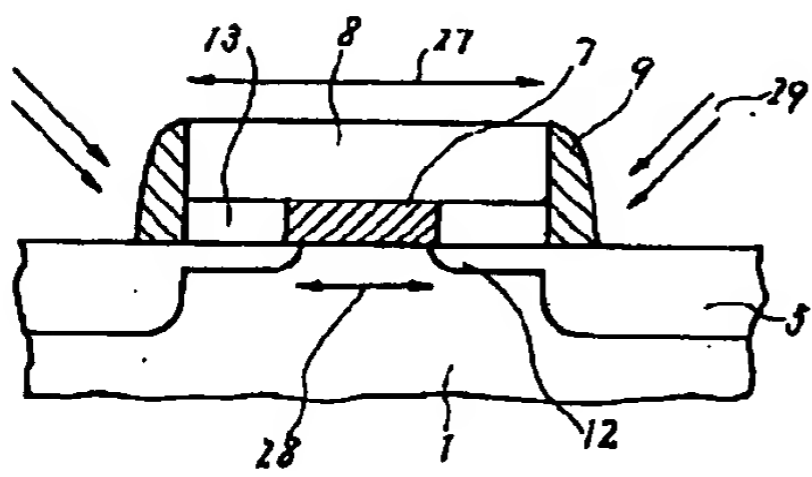
【図9】



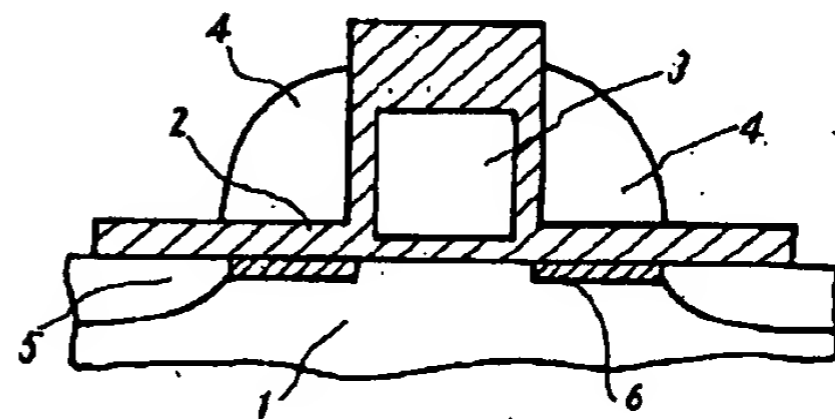
【図10】



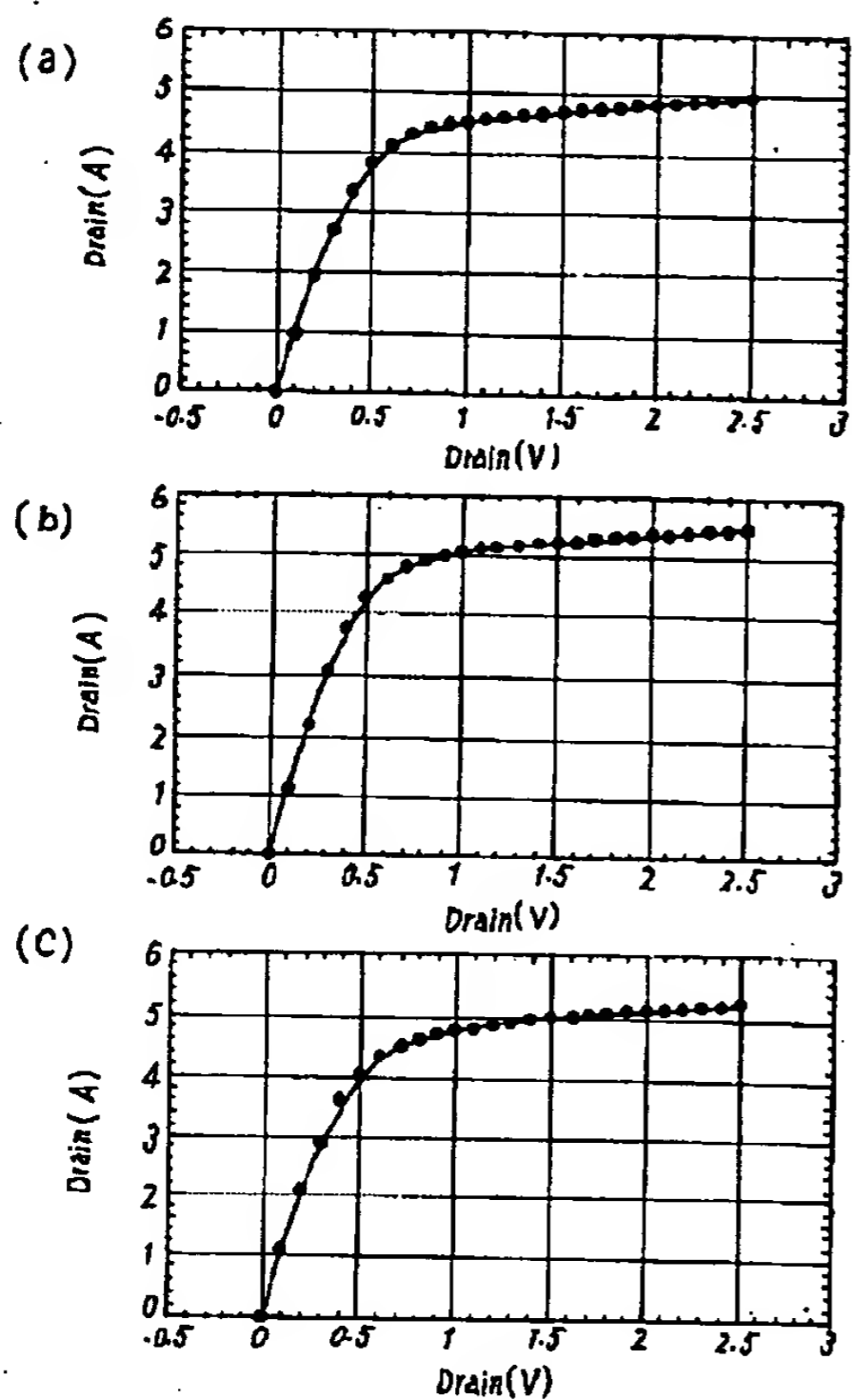
【図14】



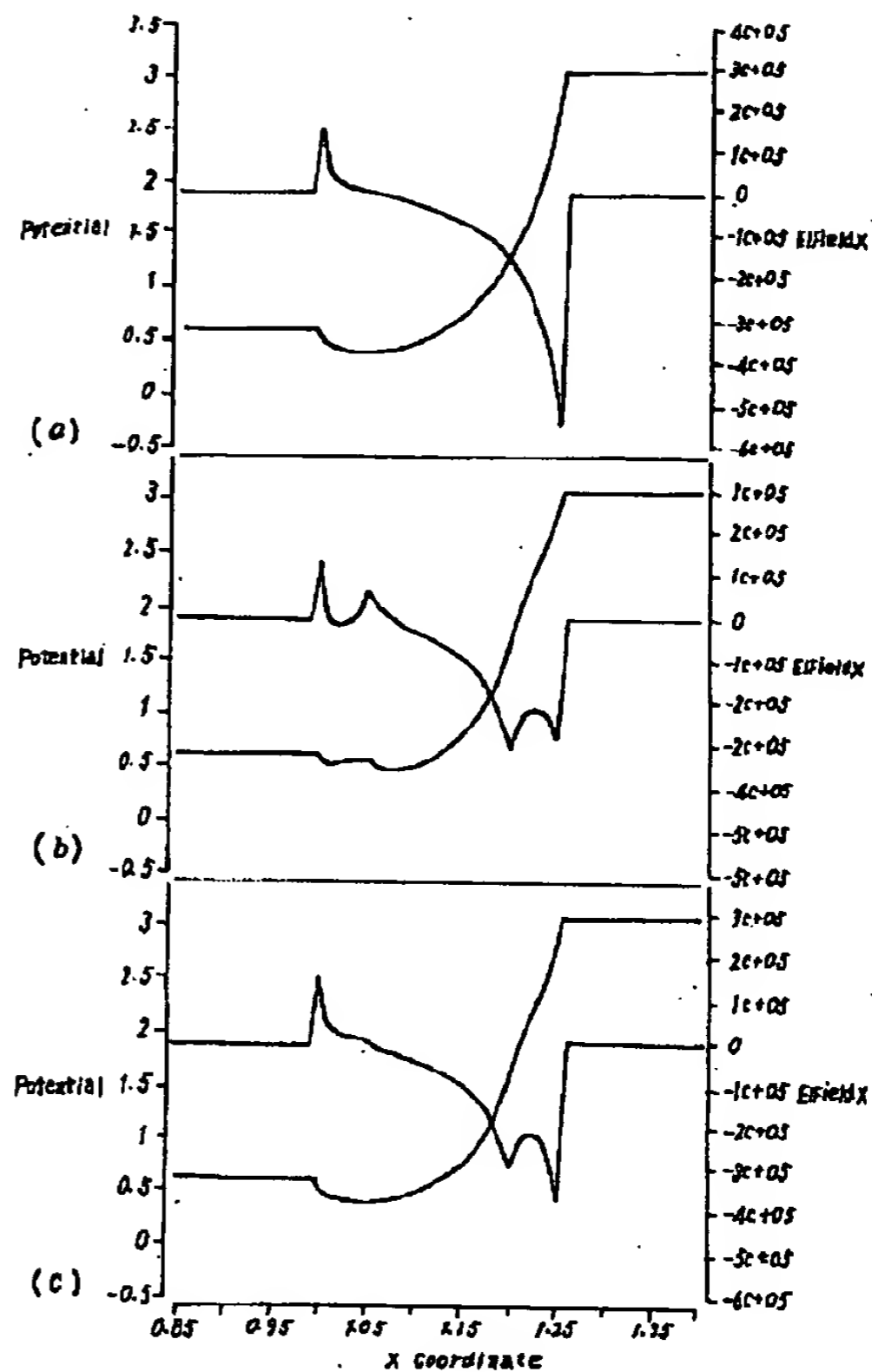
【図15】



【図11】



【図13】



**This Page is Inserted by IFW Indexing and Scanning
Operations and is not part of the Official Record**

BEST AVAILABLE IMAGES

Defective images within this document are accurate representations of the original documents submitted by the applicant.

Defects in the images include but are not limited to the items checked:

- ☒ **BLACK BORDERS**
- ☐ **IMAGE CUT OFF AT TOP, BOTTOM OR SIDES**
- ☐ **FADED TEXT OR DRAWING**
- ☐ **BLURRED OR ILLEGIBLE TEXT OR DRAWING**
- ☐ **SKEWED/SLANTED IMAGES**
- ☒ **COLOR OR BLACK AND WHITE PHOTOGRAPHS**
- ☐ **GRAY SCALE DOCUMENTS**
- ☐ **LINES OR MARKS ON ORIGINAL DOCUMENT**
- ☐ **REFERENCE(S) OR EXHIBIT(S) SUBMITTED ARE POOR QUALITY**
- ☐ **OTHER:** _____

IMAGES ARE BEST AVAILABLE COPY.

As rescanning these documents will not correct the image problems checked, please do not report these problems to the IFW Image Problem Mailbox.

THIS PAGE BLANK (USPTO)